Homework assignment 9 posted - due next Friday
Outline

- Register Transfer Notation
- List Processor Example
- Design Optimization
- Resource Utilization Charts
Register Transfer Notation
At the high-level we view these systems as a collection of state elements and CL blocks.

“RTL” is a commonly used acronym for “Register Transfer Level” description.

It follows from the fact that all synchronous digital system can be described as a set of state elements connected by combinational logic blocks.

Though not strictly correct, some also use “RTL” to mean the Verilog or VHDL code that describes such systems.
We introduce a notation for describing the behavior of systems at the register transfer level.

Can view the operation of digital synchronous systems as a set of data transfers between registers with combinational logic operations happening during the transfer.

**RT notation comprises a set of register transfers with optional operators as part of the transfer.**

Example:

\[
\begin{align*}
\text{reg}A & \leftarrow \text{reg}B \\
\text{reg}C & \leftarrow \text{reg}A + \text{reg}B \\
\text{if (start==1)} & \text{ reg}A \leftarrow \text{reg}C
\end{align*}
\]

We use “;” to separate transfers that occur on separate cycles.

Use “,” to separate transfers that occur on the same cycle.

Example (2 cycles):

\[
\begin{align*}
\text{reg}A & \leftarrow \text{reg}B, \text{reg}B \leftarrow 0; \\
\text{reg}C & \leftarrow \text{reg}A;
\end{align*}
\]
Example of Using RT Notation

ACC ← ACC + R0, R1 ← R0;
ACC ← ACC + R1, R0 ← R1;
R0 ← ACC;

- In this case: RT notation description is used to sequence the operations on the datapath.
- It becomes the high-level specification for the controller.
- Design of the FSM controller follows directly from the RT notation sequence. In this example (and most other designs) the FSM controls movement of data by controlling the multiplexor control signals.
Example of Using RT Notation

Sometimes RT Notation is used as a starting point for designing both the datapath and the control:

Example:

\[
\begin{align*}
\text{regA} & \leftarrow \text{IN}; \\
\text{regB} & \leftarrow \text{IN}; \\
\text{regC} & \leftarrow \text{regA} + \text{regB}; \\
\text{regB} & \leftarrow \text{regC};
\end{align*}
\]

From this we can deduce:

- IN must fanout to both regA and regB
- regA and regB must output to an adder
- the adder must output to regC
- regB must take its input from a mux that selects between IN and regC

What does the datapath look like?

The controller:

Control points:
1. clock enable for A register
2. clock enable for B register
3. mux control

FSM controller:
4 states (one per cycle)
List Processor Example
List Processor Example

- RT Notation gives us a framework for making high-level optimizations.

- General design procedure outline:
  1. Problem, Constraints, and Component Library Spec.
  2. “Algorithm” Selection
  3. Micro-architecture Specification
  4. Analysis of Cost, Performance, Power
  5. Optimizations, Variations
  6. Detailed Design
1. Problem Specification

- Design a circuit that forms the sum of all the 2’s complement integers stored in a linked-list structure starting at memory address 0:

- Assume: All integers and pointers are 8-bit. The link-list is stored in a memory block with an 8-bit address port and 8-bit data port, as shown below. The pointer from the last element in the list is 0. At least one node in list.

Note: We don’t assume nodes are aligned on 2 Byte boundaries.
1. Other Specifications

- **Design Constraints:**
  - Usually the design specification puts a restriction on cost, performance, power or all. We will leave this unspecified for now and return to it later.

- **Component Library:**

<table>
<thead>
<tr>
<th>component</th>
<th>delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>simple logic gates</td>
<td>0.5ns</td>
</tr>
<tr>
<td>n-bit register</td>
<td>clk-to-Q=0.5ns, setup=0.5ns</td>
</tr>
<tr>
<td>n-bit 2-1 multiplexor</td>
<td>1ns</td>
</tr>
<tr>
<td>n-bit adder</td>
<td>(2 log(n) + 2)ns</td>
</tr>
<tr>
<td>memory</td>
<td>10ns read (asynchronous read)</td>
</tr>
<tr>
<td>zero compare</td>
<td>0.5 log(n)</td>
</tr>
</tbody>
</table>

*(single ported memory, register has CE but no RST)*

Are these reasonable?
Review of Register with “Clock Enable”

- Register with Clock Enable:
  - Allows register to be either loaded on selected clock positive edge or to retain its previous value.
  - Assume both data and CE require setup time = 0.5ns.
  - Assume no reset input.

*Functional description only. Transistor level circuit could have lower input delay and fewer transistors.*
In this case the memory only allows one access per cycle, so the algorithm is limited to sequential execution. If in another case more input data is available at once, then a more parallel solution may be possible.

**Assume datapath state registers NEXT and SUM.**
- NEXT holds a pointer to the node in memory.
- SUM holds the result of adding the node values to this point.

If (START==1) NEXT←0, SUM←0, DONE←0;
repeat {
    SUM←SUM + Memory[NEXT+1];
    NEXT←Memory[NEXT];
} until (NEXT==0);
R←SUM, DONE←1;

*This RT Notation becomes the basis for DP and controller.*
Direct implementation of RTL description:

**Datapath**

If \((\text{START}==1)\) \(\text{NEXT} \leftarrow 0\), \(\text{SUM} \leftarrow 0\);
repeat  
\[
\text{SUM} \leftarrow \text{SUM} + \text{Memory}[\text{NEXT}+1];
\]
\[
\text{NEXT} \leftarrow \text{Memory}[\text{NEXT}];
\]
until \((\text{NEXT}==0)\);
\(R \leftarrow \text{SUM}, \text{DONE} \leftarrow 1;\)
4. Analysis of Cost, Performance, and Power

- Skip Power for now.

- Cost:
  - How do we measure it? # of transistors? # of gates? # of CLBs?
  - Depends on implementation technology. Often we are just interested in comparing the *relative* cost of two competing implementations. (Save this for later)

- Performance:
  - 2 clock cycles per number added.
  - What is the minimum clock period?
  - The controller might be on the critical path. Therefore we need to know the implementation, and controller input and output delay. We do a design and could later optimize if it is indeed on the critical path.
Possible Controller Implementation

- Based on this, what is the controller input and output delay?
4. Analysis of Performance

Other paths exist for each cycle in the loop. These are the worst case.

If (START==1) NEXT<-0, SUM<-0;
repeat {
  SUM<-SUM + Memory[NEXT+1];
  NEXT<-Memory[NEXT];
} until (NEXT==0);
R<-SUM, DONE<-1;

 COMPUTE_SUM state

 GET_NEXT state

D
Memory

A

18
4. Analysis of Performance

- **Detailed timing:**
  - clock period (T) = max (clock period for each state)
  - T > 31ns, F < 32 MHz

- **Observation:**
  - COMPUTE_SUM state does most of the work. Most of the components are inactive in GET_NEXT state.
  - GET_NEXT does: Memory access + …
  - COMPUTE_SUM does: 8-bit add, memory access, 15-bit add + …

- **Conclusion:**
  - Move one of the adds to GET_NEXT.
List Processor Optimization
Add new register named NUMA, for *address of number to add*.

- Update code to reflect our change (note still 2 cycles per iteration):

  ```
  If (START==1) NEXT ← 0, SUM ← 0, NUMA ← 1;
  repeat {
    SUM ← SUM + Memory[NUMA];
    NUMA ← Memory[NEXT] + 1, NEXT ← Memory[NEXT]
  } until (NEXT==0);
  R ← SUM, DONE ← 1;
  ```
5. Optimization

- Architecture #2:

  If (START==1) NEXT<-0, SUM<-0, NUMA<-1;
  repeat {
    SUM<-SUM + Memory[NUMA];
    NUMA<-Memory[NEXT] + 1, NEXT<-Memory[NEXT] ;
  } until (NEXT==0);
  R<-SUM, DONE<-1;

- Incremental cost: addition of another register and mux.
5. Optimization, Architecture #2

- New timing:
  Clock Period (T) = max (clock period for each state)

  \[ T > 23\text{ns}, \quad F < 43\text{Mhz} \]

- Is this worth the extra cost?
- Can we lower the cost?

Notice that the circuit now only performs one add on every cycle. Why not share the adder for both cycles?
5. Optimization, Architecture #3

- **Incremental cost:**
  - Addition of another mux and control (ADD_SEL). Removal of an 8-bit adder.

- **Performance:**
  - No change.

- **Change is definitely worth it.**
Resource Utilization Charts
One way to visualize these (and other possible) optimizations is through the use of a resource utilization charts.

These are used in high-level design to help schedule operations on shared resources.

Resources are listed on the y-axis. Time (in cycles) on the x-axis.

Example:

<table>
<thead>
<tr>
<th>resource</th>
<th>cycle</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>memory</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bus</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>register-file</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ALU</td>
<td></td>
<td>A1+B1</td>
<td>A2+B2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Our list processor has two shared resources: memory and adder.
Unoptimized solution: 1. $\text{SUM} \leftarrow \text{SUM} + \text{Memory}[\text{NEXT}+1]$; 2. $\text{NEXT} \leftarrow \text{Memory}[\text{NEXT}]$;

<table>
<thead>
<tr>
<th></th>
<th>fetch x</th>
<th>fetch next</th>
<th>fetch x</th>
<th>fetch next</th>
</tr>
</thead>
<tbody>
<tr>
<td>memory</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>adder1</td>
<td></td>
<td>next+1</td>
<td></td>
<td>next+1</td>
</tr>
<tr>
<td>adder2</td>
<td></td>
<td>sum</td>
<td></td>
<td>sum</td>
</tr>
</tbody>
</table>

1. $\text{SUM} \leftarrow \text{SUM} + \text{Memory}[\text{NUMA}]$;
2. $\text{NEXT} \leftarrow \text{Memory}[\text{NEXT}], \text{NUMA} \leftarrow \text{Memory}[\text{NEXT}]+1$;

<table>
<thead>
<tr>
<th></th>
<th>fetch x</th>
<th>fetch next</th>
<th>fetch x</th>
<th>fetch next</th>
</tr>
</thead>
<tbody>
<tr>
<td>memory</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>adder</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

• How about the other combination: $\text{add x register}$

<table>
<thead>
<tr>
<th></th>
<th>fetch x</th>
<th>fetch next</th>
<th>fetch x</th>
<th>fetch next</th>
</tr>
</thead>
<tbody>
<tr>
<td>memory</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>adder</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1. $X \leftarrow \text{Memory}[\text{NUMA}], \text{NUMA} \leftarrow \text{NEXT}+1$;
2. $\text{NEXT} \leftarrow \text{Memory}[\text{NEXT}], \text{SUM} \leftarrow \text{SUM}+X$;

• Does this work? If so, a very short clock period. The fetch and the add from each cycle would be independent. $T = \max(T_{\text{mem}}, T_{\text{add}})$ instead of $T_{\text{mem}} + T_{\text{add}}$. 

27
List Example Resource Scheduling - Ad hoc method

- Schedule one loop iteration followed by the next (4 cycles per result):

<table>
<thead>
<tr>
<th>Memory</th>
<th>( \text{next}_1 )</th>
<th>( x_1 )</th>
<th>( \text{next}_2 )</th>
<th>( x_2 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>adder</td>
<td>numa_1</td>
<td>sum_1</td>
<td>numa_2</td>
<td>sum_2</td>
</tr>
</tbody>
</table>

- How can we overlap iterations? \( \text{next}_2 \) depends on \( \text{next}_1 \).
  - “slide” second iteration into first (3 cycles per result):

<table>
<thead>
<tr>
<th>Memory</th>
<th>( \text{next}_1 )</th>
<th>( x_1 )</th>
<th>( \text{next}_2 )</th>
<th>( x_2 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>adder</td>
<td>numa_1</td>
<td>sum_1</td>
<td>numa_2</td>
<td>sum_2</td>
</tr>
</tbody>
</table>

- or further:

<table>
<thead>
<tr>
<th>Memory</th>
<th>( \text{next}_1 )</th>
<th>( \text{next}_2 )</th>
<th>( x_1 )</th>
<th>( x_2 )</th>
<th>( \text{next}_3 )</th>
<th>( \text{next}_4 )</th>
<th>( x_3 )</th>
<th>( x_4 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>adder</td>
<td>numa_1</td>
<td>numa_2</td>
<td>sum_1</td>
<td>sum_2</td>
<td>numa_3</td>
<td>numa_4</td>
<td>sum_3</td>
<td>sum_4</td>
</tr>
</tbody>
</table>

Initiation Interval (II) = 4
Initiation Interval (II) = 3

The repeating pattern is 4 cycles. Not exactly the pattern what we were looking for. But does it work correctly?
List Example Resource Scheduling - another attempt

- In this case, first spread out, then pack.

<table>
<thead>
<tr>
<th>Memory</th>
<th>next₁</th>
<th>x₁</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>adder</td>
<td>numa₁</td>
<td>sum₁</td>
<td></td>
</tr>
</tbody>
</table>

- Three different loop iterations active at once.
- Short cycle time (no dependencies within a cycle)
- Full utilization (only 2 cycles per result)
- Initialization: x=0, numa=1, sum=0, next=memory[0]
- Control states (out of the loop)
  - two to start: initialize next, clear sum, set numa, clear x; get next₂ two to finish:

1. X←Memory[NUMA], NUMA←NEXT+1;
2. NEXT←Memory[NEXT], SUM←SUM+X;

Initiation
Interval (II) =2
5. Optimization, Architecture #4

- **Datapath:**
  - Incremental cost:
    - Addition of another register & mux, adder mux, and control.
  - **Performance:** find max time of the four actions
    1. X ← Memory[NUMA], NUMA ← NEXT+1; 0.5+1+10+1+0.5 = 13ns
    2. NEXT ← Memory[NEXT], SUM ← SUM+X; same for all \( \Rightarrow T > 13\text{ns}, F < 77\text{MHz} \)
Other Optimizations

Node alignment restriction:
- If the application of the list processor allows us to restrict the placement of nodes in memory so that they are aligned on even multiples of 2 bytes.
  - NUMA addition can be eliminated.
  - Controller supplies “0” for low-bit of memory address for NEXT, and “1” for X.
- Furthermore, if we could use a memory with a 16-bit wide output, then could fetch entire node in one cycle:

\[
\{\text{NEXT}, \text{X}\} \leftarrow \text{Memory}[\text{NEXT}], \quad \text{SUM} \leftarrow \text{SUM} + \text{X};
\]

\[\Rightarrow\text{ execution time cut in half (half as many cycles)}\]
List Processor Conclusions

- Through careful optimization:
  - clock frequency increased from 32MHz to 77MHz
  - little cost increase.

- “Scheduling” was used to overlap and to maximize use of resources.

- Essentially through pipelining the operations (the extra added registers - NUMA, X - act as pipeline registers.

- Questions:
  - Consider the design process we went through:
    - Could a computer program go from RTL description to circuits automatically?
    - Could a computer program derive the optimizations that we did?
    - It is the goal of “High-Level Synthesis” to do similar transformations and automatic mappings. “C-to-gates” compilers are an example.